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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/685,877	10/11/2000	Yun-chan Myung	Q61029	3932

7590 06/04/2004

SUGHRUE, MION, ZINN, MACPEAK & SEAS,PLLC
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037-3202

EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/685,877	MYUNG, YUN-CHAN	
	Examiner	Art Unit	
	Nilesh R Shah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1.-13 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (5,291,614) (hereinafter Baker).

4. As per claim 1, Baker teaches a real time control system of a multitasking digital signal processor, comprising: a ready queue including a ready queue link, the ready queue link comprising a first information indicating a first task control block for a sequentially first task among tasks in the digital signal processor, and a second task control block for a sequentially last task among the tasks in the digital signal processor (col. 4 lines 5-51, col. 10 line 10-65),

a priority link group of priority links, a number of the priority links being equal to a number of priority levels of the tasks in the digital signal processor (col. 12 lines 16- 59), and

a second information indicating a third task control block for a sequentially first task among tasks having same priority among the tasks in the digital signal processor, and a fourth task control block for a sequentially last task among the tasks having same priority (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8);
and an operating system for setting the first and second information according to conditions of tasks for the digital signal processor, and controlling switching between the tasks of the ready queue (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8).

Baker does not teach the use of transferring tasks over a network.

It is well know in the art of task management to transfer tasks over a network. It should be noted that what is claimed and what is disclosed in Baker differs only in the sense that in the claimed invention, tasks are being transferred over a network, while in Baker functions are transmitted over a network. In either case, data is being transferred over a communications system, and the form or function of that data is immaterial to what the scope of the invention is. Therefore, it would have been obvious to one of ordinary skill in the art to substitute the method of transmitting functions from a TCB as in Baker for tasks or any other type of data that is to be transmitted over a communications network. The discrepancy in type of data is immaterial, and the scopes of the inventions are essentially equivalent.

5. As per claim 2 Baker teaches a real time control system wherein the first information comprises a first list pointer corresponding to the first task control block and a second pointer corresponding to the second task control block (col. 4 lines 5-51, col. 10 line 10-65), and

the second information comprises a third list pointer corresponding to the third task control block and a fourth pointer corresponding to the fourth task control block (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, Fig 8).

6. As per claim 3 Baker teaches a real time control system wherein the operating system updates the first and second information so that deterministic scheduling with respect to the ready queue link and the priority link is maintained, when a task for the digital single processor is inserted or deleted (col. 10 line 10 –col. 11 line 32).

7. As per claim 4, Baker teaches a real time control system further comprising a waiting queue including a waiting queue link, the waiting queue link comprising a third information indicating a fifth task control block for the sequentially first task among the tasks in the digital signal processor, and a sixth task control block for the sequentially last task among the tasks in the digital signal processor (col. 10 line 10 –col. 11 line 32).
a second priority link group of second priority links, a number of the second priority links being equal to the number of priority levels of the tasks in the digital signal processor;
a fourth information indicating a seventh task control block for the sequentially first task among the tasks having the same priority among the tasks in the digital signal processor,

and an eighth task control block for the sequentially last task among the tasks having the same priority; and

wherein the operating system sets the third and fourth information so that resources for the tasks of the waiting queue are deterministically acquired (col. 10 line 10 –col. 11 line 32).

8. As per claim 5, Baker teaches a real time control system wherein the third information comprises a fifth list pointer corresponding to the fifth task control block and a sixth pointer corresponding to the sixth task control block, and the fourth information comprises a seventh list pointer corresponding to the seventh task control block and an eighth pointer corresponding to the eighth task control block processor (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8).

9. As per claim 6, Baker teaches a real time control system wherein the operating system controls the ready queue so that switching between the tasks is achieved on a basis of the priority link group, when task searching in the digital signal processor is based on an order of the priority of the tasks, (col. 10 line 10 –col. 11 line 32); and
and controls the ready queue so that switching between the tasks is achieved on a basis of the ready queue link, when the task searching is based on a first-in first-out (FIFO) system. (col. 10 line 10 –col. 11 line 32).

10. As per claim 7, Baker teaches a real time control system further comprising a timer wheel for managing timer control blocks for the tasks in a pointer arrangement structure, wherein the operating system inserts the timer control blocks into corresponding slots of the timer wheel according to a time set for the tasks in the digital signal processor (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8).

11. As per claim 8 baker teaches a real time control system wherein the timer wheel is divided into two timer wheels according to a predetermined reference time, and the operating system inserts timer control blocks corresponding to slots of the first timer wheel when the time set for the tasks is equal to or less than the predetermined reference time, and inserts timer control blocks corresponding to slots of the second timer wheel when the time set for the tasks is greater than the predetermined reference time and equal to or less than twice the predetermined reference time (col. 4 lines 5-51, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8).

12. As per claim 9, Barker teaches a real time control system wherein the operating system generates errors when the time set for the tasks is greater than twice the predetermined reference time (col. 4 lines 5-51, col.9 lines 1- 45, col. 10 line 10-65, col. 12 lines 33-68, col. 13 lines 15-67, fig 8).

13. As per claim 10, Baker teaches a real time control system wherein a memory used to process the tasks in the digital signal processor is divided into an internal memory and an

external memory in the digital signal processor, and the operating system manages the internal memory and the external memory using a memory structure made up of a start address, an end address, a memory size, a memory map, and next information indicating the start address of a next memory to be connected (col. 4 lines 5-63, col. 10 line 10-65).

14. As per claim 11 Baker teaches a real time control system where in the operating system manages the memory so that the internal memory is allocated when the digital signal processor is required to perform fast processing on a task and so that the external memory is allocated when the internal memory is completely allocated (col. 4 lines 5-63, col. 10 line 10-65).

15. As per claim 12, Baker teaches a real time control system wherein the operating system manages the memory so that the external memory is divided into a plurality of memories using the memory structure (col. 4 lines 5-63).

16. As per claim 13, Baker teaches a real time control system, wherein the operating system allocates and returns the memory in units of predetermined-sized pages in a system call way, and checks allocation or non-allocation of the memory on the basis of the map of a memory (col. 4 lines 5-63).

Response to Arguments

17. Applicant's arguments filed 03/18/04 have been fully considered but they are not persuasive.

18. Applicant states Baker fails to teach:

    (a) the TMS block which obtains, stores or uses information indicative of a task control block for a sequentially last task among the tasks in its digital signal processor.

19. Examiner respectfully disagrees with applicant's remarks. First, claim 1 fails to specifically point out the following features: obtains, stores or uses information indicative of a task control block for a sequentially last task among the tasks in its digital signal processor.

    Baker clearly teaches

    (a) A control block that is based on the last task among the tasks in the digital signal processor (fig. 6, col. 9 lines 47-65, col. 10 lines 61-65, col. 11 lines 22 –32, col. 12 lines 64-68, col. 13 lines 7-14 and col. 16 lines 47-58).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

    A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh R Shah whose telephone number is 703-305-8105. The examiner can normally be reached on Monday-Friday 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

May 18, 2004
NS